

Description

Variable Capacitor Using MOS Gated Diode with Multiple Segments to Limit DC Current

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of the co-pending application for Variable Capacitor Using MOS Gated Diode with Multiple Segments to Limit DC Current , U.S. Ser. No. 09/683,709, filed 2/5/02, which is a continuation-in-part of the co-pending application for MOS Variable Capacitor with Controlled dC/dV and Voltage Drop Across W of Gate, U.S. Pat. No. 6,541,814, issued 4/1/03.

BACKGROUND OF INVENTION

[0002] This invention relates to integrated circuit capacitors, and more particularly to voltage-variable integrated capacitors.

[0003] Variable capacitors or varactors have been used for many years in tuning circuits. For example, radio receivers once

used variable capacitors that adjusted a band-pass frequency in a tuning circuit, allowing one radio station to be amplified while suppressing other radio frequency signals. The amount of capacitance was varied by a user turning a dial that rotated half of the metal plates of the capacitor. As the user rotated the plates, the overlap area between adjacent metal plates varied, thus varying the capacitance value. Figure 1A shows a symbol for a variable capacitor or varactor.

[0004] More recently, capacitors have been integrated onto larger integrated circuit (IC) chips. Often a capacitor is formed from a metal-oxide-semiconductor (MOS) field-effect transistor. Figure 1B shows a prior-art MOS capacitor. The source and drain terminals of the MOS transistor are shorted together and form one terminal ND of the capacitor, with the MOS transistor's gate forms the second capacitor terminal NG. The very thin gate oxide provides a large capacitance value in a small area.

[0005] The capacitance can be varied by changing the size of the MOS transistor. The circuit designer can select the desired capacitance by selecting the W and L values of the capacitor-transistor. However, once the circuit is manufactured, the capacitance is fixed.

[0006] A variable capacitor can be made by including several capacitors in parallel on the IC chip. An array of switches or pass transistors can selectively couple the parallel capacitors to a circuit node. Electronic signals can be applied to the gates of some of the pass transistors to electronically connect the selected capacitors to the circuit node. Other electronic signals can turn off other pass transistors, disconnecting their capacitors from the circuit node. As more of the parallel capacitors are connected to the circuit node, the capacitance increases. Thus the total capacitance attached to the circuit node can be electronically selected. The electronic signals can be coded binary signals such as a thermometer code.

[0007] While such a binary-controlled variable capacitor is useful, an analog-voltage controlled variable capacitor is desired. A variable capacitor that changes its capacitance value based on an applied voltage can allow for a wider range of capacitances, rather than a limited quanta of capacitances selected by binary control signals. What is desired is a voltage-variable capacitor that can be integrated with circuits using common MOS processes.

[0008] The parent application disclosed such an analog-controlled variable capacitor using a MOS transistor. A voltage

gradient was applied across the source and across the drain, so that the source acted as a resistor, and the drain acted as another resistor. The variable capacitance was from the gate to the channel. However, one of the two nodes of the variable capacitor was the source/drain, which also had the voltage gradient and a current flow. It is desirable to have the voltage gradient applied to a third node that is separate from the two nodes of the variable capacitor.

[0009] What is desired is to have the variable capacitance from the channel to the substrate, but under control of the gate. A variable capacitor using a gated-diode is desired.

BRIEF DESCRIPTION OF DRAWINGS

[0010] Figure 1A shows a symbol for a variable capacitor or var-actor.

[0011] Figure 1B shows a prior-art MOS capacitor.

[0012] Figure 2A shows a cross-section of a MOS transistor used as a variable capacitor.

[0013] Figure 2B shows a cross section of a gated diode used as a variable capacitor.

[0014] Figure 3 shows a MOS-transistor gated diode operating as a variable capacitor.

- [0015] Figure 4 shows grounded-lower-gate biasing of the varactor.
- [0016] Figure 5 shows above-ground lower-gate biasing of the varactor.
- [0017] Figure 6 is a graph showing variation of capacitance with source and gate voltages.
- [0018] Figure 7 is a low-current embodiment of the voltage-variable capacitor.
- [0019] Figure 8 shows the use of the variable capacitor in a voltage-controlled crystal oscillator circuit.
- [0020] Figure 9 shows the use of the variable capacitor in a L-C tuning or tank circuit.

DETAILED DESCRIPTION

- [0021] The present invention relates to an improvement in voltage-variable capacitors. The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and de-

scribed, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0022] Figure 2A shows a cross-section of a MOS transistor used as a variable capacitor. A bias voltage applied to gate 10 causes an inversion layer or channel 16 to form in substrate 18 under gate 10. This allows current to flow between drain and source 12 in a typical transistor. Substrate tap 14 is a p+ region that can be used to bias substrate 18 to ground or another potential.

[0023] In the parent application, the variable capacitance 21 was the gate-to-channel capacitance, from gate 10 to channel 16. The potential of channel 16 varied in the W direction (perpendicular to the plane of the drawing) since the potential of source 12 varied along the source. In a typical transistor, source 12 is biased to a constant potential that is the same everywhere within source 12. Unlike the typical transistor, the parent application set up a voltage gradient across the source itself, so that the source acted like a resistor.

[0024] Figure 2B shows a cross section of a gated diode used as a variable capacitor. The inventor also realizes that the voltage gradient ($V_{GH}-V_{GL}$) can be applied across the gate, with the gate acting as a resistor. Current i flows

through gate 10, from VGH to VGL. The capacitance adjusted is between channel 16 and substrate 18. Drain and source 12 set a nominal potential of channel 16. Substrate tap 14 controls the potential of substrate 18, which is typically grounded.

[0025] However, the potential of gate 10 affects channel 16. The MOS transistor acts as a gated diode, with gate 10 controlling the formation of channel 16. By placing a voltage gradient along gate 10, the channel area and capacitance can be varied. Thus the variable capacitance 21' is from channel 16 to substrate 18, but is controlled by bias voltages VGH and VGL on gate 10, and the source/drain voltage VS.

[0026] MOS Gated Diode As Variable Capacitor – Fig. 3

[0027] Figure 3 shows a MOS-transistor gated diode operating as a variable capacitor. This is a layout or overhead view showing the gate, substrate, and contact layers.

[0028] Traditionally, the same voltage is applied to all contacts of the gate. Instead, the inventor applies different voltages to the ends of gate 30. An upper voltage VGH is applied to upper contact 34, while a lower voltage VGL is applied to contact 32. Upper contact 34 connects to a metal line, which is biased to voltage VGH by a bias circuit (not

shown). Lower contact 32 connects to another metal line, which is biased to lower voltage VGL by another bias circuit.

[0029] A voltage gradient or differential of VGH–VGL is thus applied across gate 30. A current flows from upper contact 34 to lower contact 32 through gate 30, which acts as a resistor.

[0030] The size of the transistor is defined by the width W and length L of gate 30. The channel length L is the direction of normal transistor current flow under gate 30, while the width W is the direction perpendicular to current flow in a normal transistor.

[0031] The total capacitance of the varactor is the sum of the source–to–substrate junction capacitance, the drain–to–substrate junction capacitance, and the channel–to–substrate junction capacitance. The area of the source and drain junction capacitors are fixed and these components of the total capacitance vary with the source and substrate voltage difference. However, the area of the channel is a function of the gate, source, and drain voltages. When the transistor is biased in an off condition, no conducting channel forms in the substrate under gate 30, and the channel–to–substrate capacitance is near zero,

being only the parasitic and fringe capacitances. The full channel-to-substrate capacitance is available when the channel is fully formed.

[0032] Gate Voltage Varies Along W Direction

[0033] However, when a voltage difference is applied across the gate 30, the voltage under gate 30 is not constant. Instead, the voltage under gate 30 varies as a function of distance between contacts 34, 32. For portions of gate 30 that are near upper contact 34, the gate voltage is near V_{GH} . Portions of gate 30 near lower contact 32 have gate voltages near V_{GL} . The middle of gate 30, halfway between contacts 34, 32, has a gate voltage halfway between V_{GH} and V_{GL} , such as $(V_{GH}-V_{GL})/2$ when the transistor is off.

[0034] The source and drain regions 22 are connected by source contacts 36 to line 54, which is biased to a source voltage V_S that can vary somewhat but can be considered constant for purposes of analysis. For a basic understanding of the operation of the variable capacitor, assume that V_S is constant, or changes very slowly so that it can be considered constant at a point in time. The same source voltage V_S is applied to all parts of source and drain regions 22 by contacts 36 to metal lines (not shown) that are con-

nected to line 54.

[0035] Since the source voltage does not vary along the W direction of gate 30, but the gate voltage does, the gate-to-source voltage V_{gs} also varies along the W direction. For certain biasing conditions, the gate-to-source voltage can be above the threshold near upper contact 34, but below the threshold near lower contact 32. The lower portion 30A of gate 30 near lower contact 32 is turned off, since the gate-to-source voltage is below the threshold required to turn on the conducting channel under gate 30 ($V_G(Y) - V_S = V_{gs} < V_{th}$).

[0036] However, the upper portion or region 30B of gate 30 near upper contact 34 is turned on, since the gate-to-source voltage is above the threshold required to turn on the conducting channel in the substrate under gate 30 ($V_G(Y) - V_S = V_{gs} > V_{th}$). At a location where $V_G(Y) - V_S$ is exactly equal to threshold V_{th} , the channel just starts to form. This is shown as a dotted-line region between lower region 30A (transistor off) and upper region 30B (transistor on).

[0037] The variable Y is the distance from upper contact 34. Y is 0 near upper contact 34, but is W near lower contact 32. This simplified analysis assumes that upper contact 34

and lower contact 32 are at the ends of the active region under gate 30. In an actual device, there is a slight voltage drop from upper contact 34 to the upper edge of gate 30, and another voltage drop from the lower edge of gate 30 to lower contact 32. These parasitic voltage drops can be decreased by using wider and shorter polysilicon tabs to contacts 32, 34.

[0038] The channel-to-substrate capacitance is proportional to the integral of the channel-to-substrate capacitance along the Y (W) direction. The approximate capacitance is the channel-to-substrate capacitance of upper region 30B, which is proportional to the area $L \cdot Y_T$, where Y_T is Y where $V_G(Y) - V_S = V_{th}$.

[0039] Capacitance Varies with Applied Voltages

[0040] The capacitance can be varied by adjusting the biasing conditions. The source voltage V_S can be lowered to make more values of Y have gate-to-source voltages over the threshold, thus increasing the area of turned-on upper region 30B. Increasing source voltage V_S moves the threshold point Y_T higher, reducing the area of turned-on upper region 30B and thus lowering capacitance. The capacitance therefore varies with source voltage V_S . Since the capacitance varies with source voltage V_S , the device

is a voltage-variable capacitor, or varactor.

[0041] The capacitance also varies with the gate voltages. When V_{GH} or V_{GL} is raised, higher gate voltages occur everywhere, thus increasing the area of turned-on upper region 30B, and increasing the capacitance.

[0042] Substrate tap 14 is a P+ region that makes electrical contact with the p-type substrate under gate 30 and source/drain regions 22. Contacts 38 can be connected to a substrate-bias voltage, such as ground.

[0043] While the capacitance from the gate to the channel varies with gate and source voltages, the variable capacitor uses the channel-to-substrate capacitance, rather than the gate-to-channel capacitance. However, the channel-to-substrate capacitance is a function of the size of the channel, and thus also varies with gate voltages V_{GL} , V_{GH} and source voltage V_S . The device can be connected as a variable capacitor to an external circuit by connecting the external circuit between terminal 40 of line 54 and the substrate. Since the substrate is often grounded, the external circuit can simply connect to line 54, and have a variable capacitance to ground.

[0044] Grounded Lower Contact – Fig. 4

[0045] Figure 4 shows grounded-lower-gate biasing of the var-

actor. In this embodiment, the same physical transistor structure can be used as shown for Fig. 3. The substrate is biased to ground by contacts 38 in substrate tap 14.

Lower gate voltage VGL is grounded, while upper gate voltage VGH is above ground.

[0046] Lower contact 32 of gate 30 is grounded, while upper contact 34 is connected to variable voltage source 44 by a metal line. Variable voltage source 44 could be a variable-voltage generated from a battery and a variable resistor, or by some other voltage-generating circuit. For example, a digital-to-analog converter (DAC) could receive a binary code and convert it to variable voltage VGH.

[0047] Source/drain regions 22 are biased with voltage VS through contacts 36. The source voltage VS can be generated by an applied voltage from external battery 42, or from a bias-voltage generator such as a voltage divider or band-gap voltage reference. The source voltage VS could also be generated by an external circuit that uses the device as a variable capacitor. In that case, external battery 42 is not needed and can be deleted.

[0048] The capacitance from the channel to the substrate is varied as the area of the channel is changed by the adjustable upper gate voltage VGH. The channel is electri-

cally connected to drain/drain regions 22. The variable capacitance is provided to another circuit (not shown) by terminal 40 attached by line 54 to source/drain regions 22. The circuit sees a variable capacitor between terminal 40 and ground. The value of the capacitance is adjusted by varying the upper gate voltage V_{GH} using variable voltage source 44. In another embodiment, V_{GH} is fixed while V_S is the variable voltage.

[0049] Lower Gate Contact Above Ground – Fig. 5

[0050] Figure 5 shows above-ground lower-gate biasing of the varactor. In this embodiment, the same physical transistor structure can be used as shown for Fig. 3. The substrate is biased to ground by contacts 38 in substrate tap 14. Source/drain regions 22 are biased with voltage V_S through contacts 36. Lower gate voltage V_{GL} is biased above ground, while upper gate voltage V_{GH} is above ground and above V_{GL} . Upper contact 34 is connected to variable voltage source 44 by a metal line.

[0051] Since the transistor threshold voltage V_{th} is typically above ground, the size of the turned-off lower region of gate 30 is always non-zero when lower contact 32 is grounded. Since this turned-off region does not contribute to the capacitance, it is a wasted area. Since a typi-

cal transistor threshold voltage V_{th} is 0.5 to 0.7 volt, a significant part of gate 30 may be below threshold and off, even when upper gate voltage V_{GH} is raised.

[0052] To reduce the size of the turned-off region under gate 30, lower gate voltage V_{GL} can be biased above ground to near the threshold voltage. External bias 46 generates a bias voltage of about the threshold voltage, or 0.7 volt, to apply to lower contact 32. This external bias 46 could be generated by an on-chip bias-voltage generator or voltage divider, or could be generated by an external battery or power source, or could be a resistor between lower contact 32 and ground.

[0053] The source voltage V_S could be varied by adjusting the voltage of external battery 42 or using an adjustable bias generator. The value of source voltage V_S can be a voltage from ground to the power-supply voltage, when the upper gate voltage V_{GH} is connected to the power supply, such as 3.3 volts. However, when the source voltage V_S is above V_{GH} , no channel is formed and the variable capacitor stops operating as desired.

[0054] Figure 6 is a graph showing variation of capacitance with source and gate voltages. The lower gate voltage V_{GL} is fixed. As upper gate voltage V_{GH} is raised with the tran-

sistor on, the channel-to-substrate capacitance increases as a larger channel is formed. The increase in capacitance is linear with gate voltage above threshold, since more and more of the gate is turned on as the gate-to-source voltages are raised. This capacitance includes the source-to-substrate and drain-to-substrate capacitances as well as the channel-to-substrate capacitance under the gate. The turned-on upper region 30B is enlarged as the threshold point YT moves downward with the increase in gate voltage. Higher source voltages decreases the gate-to-source voltages and thus reduces the area of the channel, reducing capacitance.

[0055] Low-Current Capacitor – Fig. 7

[0056] Figure 7 is a low-current embodiment of the voltage-variable capacitor. A disadvantage of the embodiments of Figs. 3–5 is that current flows from upper contact 34 to lower contact 32 through the resistor of gate 30, For example, a 100-ohm gate resistance draws a current of 10 mA when VGH is 1 volt. The current can be reduced by using a longer, narrower gate. A 3 by 300 micron gate has 100 squares, or 2K-ohm resistance. A VGH of 1 volt then draws only 0.5 mA. Thus the current through the gate can be reduced by layout.

[0057] The gate current can be reduced by dividing the gate into several arms separated by source/drain regions 22. The gate is divided into separate gate arms 302, 304, 306, 310, 312, each having a contact 34, 33, 32 to a different bias voltage.

[0058] All gate arms can be formed in the same thin-oxide or diffusion area as source and drain regions 22. All gate arms 302, 304, 306, 310, 312 can be formed from the same polysilicon or other gate material and are connected to metal lines by contacts 32, 33, 34, which are over field oxide. Alternatively, contacts 32–34 can be eliminated by forming resistors 90 out of polysilicon, and using polysilicon to connect gate arms 203–312 to resistors 90 or to voltage biases generated in some other manner.

[0059] Each of the gate arms 302–312 has a bias voltage applied. The bias voltages are stepped in increments between the lower gate voltage V_{GL} and the upper gate voltage V_{GH} . Upper gate arm 302 is connected to V_{GH} by upper contact 34, while lower gate arm 312 is connected to V_{HL} by lower contact 32.

[0060] Intermediate gate arms are biased to intermediate voltages V_1 , V_2 , V_3 , V_4 ... These intermediate voltages can be in equal steps or divisions of the overall voltage difference

VGH–VGL. For an example with 4 intermediate voltages V1–V4 (six gate arms including the upper and lower arms) there are 5 increments. Each increment can be one–fifth of VGH–VGL. For example, when VGH is 2.0 volts and VGL is 0 volts, V1 is 0.4 volt, V2 is 0.8 volt, V3 is 1.2 volt, and V4 is 1.6 volt.

[0061] A voltage divider with many outputs, such as is formed by resistors 90 between VGH and VGL, or other voltage generators could be used to generate the intermediate voltages from VGH and VGL. While the voltage divider might draw some current, it can be designed to minimize current while still generating the intermediate voltages. Since each gate arm is separated from adjacent gate arms, there is no D.C. current path from VGH to VGL through the gates. Each gate arm is biased to a static voltage with little or no current loss.

[0062] Non–equal increments could also be substituted to vary the slope of the dC/dV curve, and the width or length of each arm could be varied, as could the number of arms. Many more arms could be used for smother capacitance adjustments.

[0063] Source/drain regions 22 are connected together by source contacts 36. Both the source and drain are connected by

contacts 36 to line 54, which is connected to capacitor terminal 40. The source voltage V_S can be applied by the external circuit, or by a bias generator or battery. Since both the drain and the source are biased to the same voltage, no drain-to-source current flows.

[0064] The capacitance seen at terminal 40 is adjusted by adjusting the upper gate bias V_{GH} . Increasing V_{GH} increases the gate-to-source voltage for all gate arms, causing more arms to exceed the transistor threshold and turn on. With more of the gate arms turned on with a conducting channel under their gate regions, the overall channel-to-substrate capacitance of the variable capacitor increases with gate voltage V_{GH} . The lower gate voltage V_{GL} could also be varied.

[0065] The capacitance may increase in discrete steps as the gate voltage is increased more than a threshold above the source voltage of the next gate arm, turning its channel on. The dC/dV curve may show steps rather than a smooth curve. This can be an advantage for some applications. For example, the circuit attached to terminal 40 may have an A.C. component that is applied to terminal 40. This A.C. component can add voltage variations to source voltage V_S . If these variations are less than the

voltage required to turn on the next arm, or turn off the uppermost arm that is on, then the A.C. variations do not change the capacitance. For the embodiment of Fig. 4, these small A.C. variations do change the capacitance as the size of the channel is varied by the A.C. variations. Thus using discrete capacitance steps provides a more stable capacitance that is still adjustable. For an embodiment with many gate arms, such as 50 gate arms, the discrete steps may merge into a smooth curve.

[0066] Use of Varactor in Circuits – Figs. 8, 9

[0067] Figure 8 shows the use of the variable capacitor in a voltage-controlled crystal oscillator circuit. Crystal 84 oscillates at a certain frequency. Amplifier 80 and resistor 82 provide feedback across the terminals of crystal 84 to induce oscillation. Battery 91 or another voltage source provides a gate bias voltage V_{GH} to variable capacitors 92, 94 through resistors 96, 98, respectively. The bias from battery 91 can be adjusted to vary the source and drain bias of variable capacitors 92, 94, thus adjusting their capacitances. Fixed capacitors 86, 88 couple variable capacitors 92, 94 to the terminals of crystal 84. This embodiment shows a common Pierce series crystal oscillator. Feedback resistor 82 keeps amplifier 80 in a high gain region. Am-

plifier 80 provides sufficient gain while the two capacitors 92 and 94 together with amplifier 80 shift phase enough to get positive feedback through crystal. When the values of variable capacitors 92 and 94 change, the phase shift due to these changes causes the crystal to change the frequency to match the phase shift, producing positive feedback.

[0068] Variable capacitors 92, 94 can be similar to the embodiment shown in Fig. 4, except that the source/drain voltage rather than the gate node is voltage-adjusted to adjust the capacitance. The terminals of the variable capacitor are ground and the source/drain node (terminal 40). The source and drain node of each variable capacitor 92, 94 is connected to the adjustable gate bias of battery 91 through resistors 96, 98. The capacitance of variable capacitor 92 in series with capacitor 96 is thus adjusted by battery 91. Likewise, the capacitance of variable capacitor 94 in series with capacitor 98 is also adjusted by battery 91.

[0069] Figure 9 shows the use of the variable capacitor in a L-C tuning or tank circuit. Inductor 100 is in parallel with a series capacitance of fixed capacitor 102 and variable capacitor 104. The resonant frequency across inductor 100

is tunable by adjusting the capacitance of variable capacitor 104.

[0070] Adjustable voltage source 108 applies a gate bias voltage VGH to variable capacitor 104 through resistor 106. This bias voltage VGH adjusts the capacitance of variable capacitor 104. Variable capacitor 104 can be the variable capacitor shown in Fig. 4, where the adjustable bias voltage is applied to the upper gate contact.

[0071] ALTERNATE EMBODIMENTS

[0072] Several other embodiments are contemplated by the inventor. For example the substrate could be biased by a charge pump to a voltage other than ground. The external circuit uses the variable capacitor by connecting between line 54 and this substrate voltage. For example, the substrate could be biased to -3 volts, and the variable capacitor has a lower terminal at -3 volts. In an actual device layout, the source side can be used by itself without a drain side, or vice-versa. Using many metal contacts reduces resistance, but is not essential.

[0073] The terms source and drain are often used interchangeably, as a source/drain region can function as a source or a drain depending on the applied bias voltages. The source and drain regions do not have to have identical

layouts or identical voltages. The drain can be biased to different voltages, although some current can flow from drain to source when the source and drain voltages are not equal. The variable capacitor could have only a source and no drain, such as by having the gate extend to field oxide where the drain would be. The drain could also be left floating, or the source and drain could be connected together by a diffusion link rather than a metal link. A p-channel transistor rather than an n-channel transistor could be substituted with appropriate changes in biases.

[0074] Many second-order effects can be taken into account using computer simulations, such as a variation of threshold V_{th} with source voltage (body effect), sub-threshold channel capacitance near V_{th} , current crowding around the edges of the source and drain regions, fringe capacitances, source-to-substrate and drain-to-substrate parasitic capacitances, and contact placement and resistances at the ends of the gate before beyond the contacts. The exact capacitance values can also be determined empirically by simply building one or more varactors, perhaps with different geometries, and measuring its capacitance for various biasing conditions. Another way of adjusting the C-V curve is by adjusting the relative resistance value

of resistors between gate arms.

[0075] The external circuit using the variable capacitor can be integrated on the same chip with the variable capacitor, or it can be on a different chip. The physical layout ordering of the gate arms does not have to follow the bias order. The gate arms can be arranged in any order, including random. Separate P+ substrate taps 14 could be used rather than an elongated tap as shown.

[0076] Other insulators besides field oxide can be used, such as trench isolation or silicon-on-insulator or non-silicon materials. Special processing steps can be eliminated since the variable capacitor is formed using standard transistor processing steps.

[0077] The abstract of the disclosure is provided to comply with the rules requiring an abstract, which will allow a searcher to quickly ascertain the subject matter of the technical disclosure of any patent issued from this disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

37 C.F.R. §1.72(b). Any advantages and benefits described may not apply to all embodiments of the invention. When the word "means" is recited in a claim element, Applicant intends for the claim element to fall under 35 USC § 112,

paragraph 6. Often a label of one or more words precedes the word "means". The word or words preceding the word "means" is a label intended to ease referencing of claims elements and is not intended to convey a structural limitation. Such means-plus-function claims are intended to cover not only the structures described herein for performing the function and their structural equivalents, but also equivalent structures. For example, although a nail and a screw have different structures, they are equivalent structures since they both perform the function of fastening. Claims that do not use the word means are not intended to fall under 35 USC § 112, paragraph 6. Signals are typically electronic signals, but may be optical signals such as can be carried over a fiber optic line.

[0078] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.